K16P 0818

Reg. No. : .....

Name : .....

II Semester M.C.A. Degree (Reg./Supple./Improve.) Examination, July 2016
(2014 Admn. Onwards)
MCA 2C09 : COMPUTER ORGANIZATION

Time : 3 Hours Max. Marks : 80

SECTION – A

Answer **any ten** questions. **Each** question carries **three** marks.

1. What are the significant features of 1's and 2's compliments ?
2. Mention the merits of stacks and sub-routines.
3. What are the functions of processor control registers ?
4. What are the operation of a microprogrammed control unit ?
5. List out the merits of instruction queue.
6. Compare the features of single bus and multibus architecture.
7. What are the merits and limitations of fast multiplication ?
8. What are the roles of cache memory in PC system ?
9. What are the significance of memory interleaving ?
10. What are the differences between I/O program controlled transfer and DMAtransfer ?
11. What are the significant features of hardware multithreading ?
12. List out the merits of superscalar operations. **(10×3=30)**

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SECTION – B

Answer **all** questions. **Each** question carries **ten** marks.

13. a) With suitable examples discuss briefly number representation and character representation of basic computer system.

OR

b) List out various addressing modes, explain any five of them briefly.

14. a) Discuss the importance of controlling I/O device behavior and processor control registers in specific task execution.

OR

b) List out various interconnection standards of I/O organization, explain any two of them briefly.

15. a) With schematic diagram discuss the operations of microprogrammed control unit.

OR

b) Explain Booths algorithm for multiplication and division operations with suitable examples.

16. a) Explain the architecture and working of virtual memory.

OR

b) Describe the functions, merits of DMA controller.

17. a) Explain the procedure involved in RISC pipelining, discuss the optimization techniques used in RISC pipelining.

OR

b) What are the various types of instruction issue policies used for instruction level parallelism and machine parallelism ?

(5×10=50)

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